10-Fold-Stack Multilayer-Grown Nanomembrane GaAs Solar Cells

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Supporting Information

ABSTRACT: Multilayer-grown nanomembrane GaAs represents an enabling materials platform for cost-efficient III–V photovoltaics. Herein we present for the first time 10-fold-stack ultrathin (emitter + base: 300 nm) GaAs solar cells. Photovoltaic performance of 10-fold-stack GaAs solar cells exhibited promising uniformity, with only slight efficiency degradation, where comparatively poor short-wavelength response was mainly responsible for the slightly reduced performance in early grown materials. Secondary ion mass spectrometry revealed the concentration of p-type dopant has been changed due to the out-diffusion of beryllium, while the extent of diffusion increasingly diminished in early grown stacks because of the reduced concentration gradient as well as the decrease of beryllium diffusivity at longer annealing times. It is therefore concluded that the performance degradation in 10-fold-stack GaAs solar cells does not develop continuously throughout the growth, but instead becomes spontaneously saturated at longer growth times, providing promising outlook for the practical application of multilayer epitaxy toward cost-competitive GaAs solar cells.

KEYWORDS: III–V solar cells, nanomembrane, ultrathin gallium arsenide, multilayer epitaxial assemblies, transfer printing

Galium arsenide (GaAs) is one of the most promising materials candidates for high efficiency photovoltaic systems owing to a number of unique advantages, including direct bandgap, ideal absorption band against solar spectrum, and superior photophysical properties, as well as established growth technology for single-crystalline materials.1−5 While GaAs-based single-junction solar cells currently have the record-high efficiency, the prohibitive cost of preparing device-quality epitaxial materials has prevented them from being widely deployed in residential photovoltaic applications where silicon-based solar cells are currently predominant.6−9 Given such compelling advantages, tremendous research efforts have been devoted over the past decades for identifying alternative routes to economically prepare high quality GaAs solar cells.8−10

Among various approaches pursued including epitaxial liftoff (ELO)8,11 and hydride vapor phase epitaxy (HVPE),12−14 growing multiple layers of solar cells on a single growth substrate, in conjunction with sequential liftoff via transfer printing, has been of special interest due to its ability to circumvent critical limitations of conventional ELO, where an excessively large number (e.g., >500) of substrate reuses is mandatory to attain cost-competitiveness.7 Critically, multilayer epitaxy has potential to significantly lower the cost of materials growth by aggressively reducing the contribution from equipment depreciation7; the time-consuming load–unload procedure is performed just once for many device growths, which is not achievable in conventional ELO or HVPE. In the pioneering work by Yoon and co-workers, triple-stack GaAs solar cells grown by metal organic vapor phase epitaxy (MOVPE) were investigated to examine the feasibility of multilayer epitaxy, where zinc and carbon were used as the p-type dopant for n-on–p and p-on–n type single-junction GaAs solar cells, respectively.15,16 In both studies, moderate performance degradation in the middle and bottom layer devices was observed primarily because of the diffusion of p-type dopant (for Zn-doped) and increases of point defects (for C-doped), respectively. More recently, Gai et al. introduced ultrathin (emitter + base: ~300 nm) device configuration into multilayer epitaxy to minimize the adverse effects of the extended thermal soaking in early grown materials and therefore allow excellent uniformity (<3% relative) of photovoltaic performance.17 Despite such optically thin absorber layers, bifacial nanophotonic light management employing hexagonally periodic TiO2 nanoposts and vertical p-type metal contact serving as a back-surface reflector enabled 17.2% one-sun efficiency from 420 nm-thick single-junction GaAs solar cells.17,18

Motivated by the successful outcome, herein we investigated 10-fold-stack (i.e., composed of 10 device layers) ultrathin GaAs solar cells for the first time to assess the possibility to accommodate massive numbers (e.g., ~100) of device stacks in multilayer epitaxy and to elucidate...
the evolution of materials properties and resulting device performance under the prolonged growth conditions. In the following, we present systematic studies of electrical, optical, and morphological properties of multilayer-grown ultrathin GaAs solar cells in 10-fold-stack epitaxial assemblies, together with thermally driven changes in dopant profiles as well as photovoltaic performance characteristics, revealing the underlying materials science and design rules for the reported system.

10-Fold-stack, n-on-p type ultrathin GaAs solar cells were grown on a (100) GaAs substrate by molecular beam epitaxy (MBE). A single-junction GaAs solar cell at each device stack consists of n-type GaAs top contact (200 nm, Si-doped, 5 × 10^{18} cm^{-3}), n-Al_{0.1}Ga_{0.9}As window (20 nm, Si-doped, 2 × 10^{18} cm^{-3}), n-GaAs emitter (50 nm, Si-doped, 2 × 10^{18} cm^{-3}), p-GaAs base (250 nm, Be-doped, 3 × 10^{17} cm^{-3}), p^{+}-Al_{0.1}Ga_{0.9}As back surface field (BSF; 50 nm, Be-doped, 5 × 10^{18} cm^{-3}), and p^{+}-GaAs bottom contact (50 nm, Be-doped, 1 × 10^{19} cm^{-3}. Figure 1a). Cross-sectional scanning electron microscope (SEM) image (Figure 1b) shows defect-free epitaxial layers of 10-fold-stack GaAs solar cells, where 400 nm-thick sacrificial layers (Al_{0.1}Ga_{0.9}As) were inserted between respective device stacks to facilitate their sequential lift-off from the growth substrate and printing-enabled integration on foreign substrates. In total, the materials growth took ~20 h, meaning that the first-grown device stack experienced thermal soaking of ~18 h at 610 °C.

Implementing ohmic or rectifying metal contact is a key requirement for high efficiency photovoltaic devices. Accordingly, contact properties such as contact resistance ($R_c$) and specific contact resistivity ($\rho_c$) were first examined by a standard transmission length method (TLM) in n-type (Pd/Ge/Au) and p-type (Pt/Ti/Pt/Au) metal contacts made on 1st, 5th, 7th and 10th device stacks. For characterization of early grown (i.e., 2nd–10th) device stacks, overlying epitaxial layers were intentionally removed by wet chemical etching as in our previous works. As summarized in Figure 1c,d and Table 1, perfect ohmic characteristics were obtained for both n- and p-type contacts in all device stacks after the thermal annealing (175 °C, 1 h under N_2). N-type metal contacts exhibited a comparable range of contact resistance and specific contact resistivity among different device stacks, while p-type contact properties progressively degraded from first to 10th layers due to the out-diffusion of beryllium during the growth of overlying stacks and resultant decrease of effective dopant concentration in the p^{+}-GaAs contact layer.

To further elucidate the effect of multilayer epitaxy on the evolution of material properties, dopant profiles of 10-fold-stack GaAs solar cells were studied by secondary ion mass spectrometry (SIMS) with as-grown epitaxial materials before further processing. In multilayer epitaxy, early grown device stacks are subject to the extended heat treatment during the growth of overlying layers, resulting in thermally activated diffusion of dopants and noticeable deviation from the optimized electronic configuration. One important question is whether the diffusion-related degradation will continually proceed with the increasing number of device stacks grown. Figure 2a and c shows SIMS concentration profiles of silicon and beryllium obtained from 1st (red), 5th (blue), 7th (green), and 10th (orange) device stacks, respectively, where the data from 5th, 7th, and 10th layers were rearranged on the same depth (x-axis) coordinate as the first layer (i.e., all profiles start from the top contact layer) such that the spatial variation of dopant concentration at constituting layers of solar cells can be easily compared among different device stacks. The thickness-averaged concentrations of silicon and beryllium extracted from the SIMS data are shown in Figure 2b and d, respectively. The average concentration of silicon in the top contact layer (i.e., n^+ GaAs) was maintained nearly constant throughout all device stacks, consistent with the uniform n-type contact properties (Figure 1c). The slight increase of silicon dopant concentrations in the top contact layers (2nd–10th) results in a gradual increase of specific contact resistivity in low-index device layers.

Table 1. Average Values of Contact Resistance and Specific Contact Resistivity for n- (Pd/Ge/Au = 5/35/80 nm) and p-Type (Pt/Ti/Pt/Au = 10/40/10/80 nm) Metal Contacts on GaAs for 1st, 5th, 7th, and 10th Device Layers

<table>
<thead>
<tr>
<th>Layer</th>
<th>1st</th>
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<th>7th</th>
<th>10th</th>
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<tbody>
<tr>
<td>n-type</td>
<td>3.8</td>
<td>5.6</td>
<td>3.1</td>
<td>5.8</td>
</tr>
<tr>
<td>p-type</td>
<td>1.3 × 10^{-4}</td>
<td>1.8 × 10^{-4}</td>
<td>4.9 × 10^{-4}</td>
<td>1.8 × 10^{-4}</td>
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Figure 2. Concentration profiles of (a) silicon and (c) beryllium with as-grown 10-stack GaAs solar cells obtained from SIMS for 1st (red), 5th (blue), 7th (green), and 10th (orange) device layers, where the concentration profiles of 5th, 7th, and 10th layers were plotted on the same depth coordinate as the 1st layer for comparison. Corresponding average concentration of (b) silicon in the emitter and top contact layers and (d) beryllium in the base and bottom contact layers, extracted from the SIMS data.

concentration in the base layer of early grown stacks attests some tendency for silicon diffusion in GaAs under the current growth condition of MBE. As expected, the extent of dopant migration was more pronounced with beryllium due to its high diffusion coefficient associated with substitutional-interstitial diffusion mechanisms,\textsuperscript{21}–\textsuperscript{23} while the profile change is comparatively less severe than zinc.\textsuperscript{22} Consequently, the concentration of beryllium in the bottom contact layer substantially decreased in long annealed stacks, while it increased in the base and emitter. The “pile-up” of beryllium near the junction seen in Figure 2c is caused by lower diffusivity of beryllium in n-GaAs due to the electric field effect with the positively charged beryllium interstitials, similar to what was reported by Enquist et al.\textsuperscript{24} The reduced beryllium concentration in the bottom contact layer directly translated to the degradation of p-type contact properties in early grown device stacks. It is also noteworthy that the rate of concentration variation was largest between first and second device stacks (Figure S1), while the layer-to-layer discrepancy gradually diminished in long-annealed stacks, which is understandable given that the concentration gradient becomes progressively smaller as the diffusion proceeds. The more uniform beryllium profile in long-annealed device stacks may also be partially explained by the phenomenon of decreasing diffusivity of beryllium with annealing time, associated with the change of nonequilibrium point defect concentrations as observed previously in MBE-grown GaAs.\textsuperscript{25}

Figure 3a shows representative current density ($J$)–voltage ($V$) curves of solar cells fabricated from 1st, 5th, 7th, and 10th device layers, measured on the wafer under simulated AM1.5G solar illumination on the source wafer. For devices from 5th, 7th, 10th layers, overlying epitaxial layers were intentionally removed by wet chemical etching such that the top contact of the target device layer is exposed to the surface as a starting point of fabrication. (b) Short-circuit current density ($J_{sc}$), fill-factor (FF), open-circuit voltage ($V_{oc}$), and efficiency ($\eta$) extracted from $JV$ characteristics in (a). Error bars indicate maximum and minimum values. (c) Semilog plots of representative dark IV curves of GaAs solar cells from 1st, 5th, 7th, and 10th device layers, measured on the source wafer (solid line). (d) reverse-bias saturation current ($−\log I_0 (A)$), diode ideality factor ($n$), series ($R_s (\Omega)$), and shunt ($R_{sh} (\Omega \cdot cm^2)$) resistances, extracted from dark IV curves. Error bars indicate maximum and minimum values.

characteristics including short-circuit current density ($J_{sc}$), open-circuit voltage ($V_{oc}$), fill factor (FF), and solar-to-electric energy conversion efficiency ($\eta$) are also summarized in Figure 3b and Table 2. As expected, the efficiency was highest at the top (1st) device stack that did not undergo any postgrowth annealing, but slightly degraded in all early grown layers, where the difference between first and 10th stacks is $\sim$11% (relative). Based on our previous works,\textsuperscript{17,18} these cells would be expected to yield $\sim$12–14% efficiency with bifacial nanoscale photon management. Notably, such performance degradation was not continuously aggravated but rather saturated with the increase of thermal soaking at early grown stacks, matching with the trend in dopant profiles. The decrease in $V_{oc}$ suggests that the degree of carrier recombination increased in early grown materials possibly due to the unintentional degradation of ultrathin ($\sim$20 nm) Al$_0.4$Ga$_0.6$As window layer (e.g., during the etching of top contact layer). Slightly reduced fill factor might be attributed to the increased series resistance associated with the elevation of emitter resistance associated with the carrier compensation due to the beryllium diffusion as well as the degraded p-type contact properties. Such characteristics of $V_{oc}$ and FF are also captured in dark IV measurements as summarized in Figures 3c,d and S2 and Table 3. Reverse bias saturation current ($I_0$) of solar cells significantly increased at fifth, seventh, 10th layers compared to the first layer device, consistent with the degradation of $V_{oc}$. It is also shown that series resistance increased while shunt resistance decreased at early grown devices, supporting the degrading trend of FF. While the lower performance of early grown devices must be
Table 2. Average Values of Short-Circuit Current Density ($J_{sc}$), Fill-Factor (FF), Open-Circuit Voltage ($V_{oc}$), and Efficiency ($\eta$) Extracted from $JV$ Characteristics in Figure 3a

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<tr>
<td>$V_{oc}$ (V)</td>
<td>0.952</td>
<td>0.914</td>
<td>0.908</td>
<td>0.919</td>
</tr>
<tr>
<td>FF</td>
<td>0.790</td>
<td>0.755</td>
<td>0.751</td>
<td>0.767</td>
</tr>
<tr>
<td>$J_{sc}$ (mA/cm²)</td>
<td>11.2 (11.2)</td>
<td>11.8 (11.9)</td>
<td>11.1 (11.2)</td>
<td>10.7 (10.8)</td>
</tr>
<tr>
<td>$\eta$ (%)</td>
<td>8.5</td>
<td>8.2</td>
<td>7.6</td>
<td>7.5</td>
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The values of $J_{sc}$ in the parentheses were derived from the EQE spectra. Maximum (Err.+) and minimum (Err.–) values of the error from the average (Avg.) are also shown.

Table 3. Average Values of Reverse-Bias Saturation Current ($\log i_{s}$ (A)), Diode Ideality Factor ($n$), Series ($R_s$ (Ω)), and Shunt ($R_m$ (Ω·cm²)) Resistances, Extracted from Dark IV Curves

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<th>10th</th>
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<tbody>
<tr>
<td>$-\log i_{s}$ (A)</td>
<td>13.1</td>
<td>11.4</td>
<td>11.5</td>
<td>11.2</td>
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<tr>
<td>$n$</td>
<td>1.919</td>
<td>2.243</td>
<td>2.212</td>
<td>2.337</td>
</tr>
<tr>
<td>$R_s$ (Ω)</td>
<td>297.8</td>
<td>645.4</td>
<td>616.6</td>
<td>408.0</td>
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<tr>
<td>$\log R_m$ (Ω·cm²)</td>
<td>8.0</td>
<td>6.9</td>
<td>7.0</td>
<td>6.6</td>
</tr>
</tbody>
</table>

“Maximum (Err.+), and minimum (Err.–) values of the error from the average (Avg.) are also shown.

Figure 4. (a) Internal (IQE) and external (EQE) quantum efficiencies, and specular reflectance ($R$) spectra measured from 5th, 7th, and 10th device layers, measured on the as-grown wafer. (b) Comparison of short-circuit current densities derived using QE spectra and directly measured from $JV$ curves.

For MBE growth, GaAs substrate was heated up to 650 °C for deoxidation and reduced to 610 °C before the growth began. A buffer layer of 200 nm GaAs (1 μm/h, V/III = 15, unintentionally doped) was then grown, followed by the growth of 400 nm Al$_{0.5}$Ga$_{0.5}$As (0.5 μm/h, V/III = 50, unintentionally doped), 50 nm p'-GaAs (0.5 μm/h, V/III = 25, Be-doped, 1 × 10¹⁹ cm⁻³), 50 nm p'-Al$_{0.5}$Ga$_{0.5}$As (0.71 μm/h, V/III = 20, Be-doped, 5 × 10¹⁸ cm⁻³), 250 nm p-GaAs (1 μm/h, V/III = 15, Be-doped, 3 × 10¹⁷ cm⁻³), 50 nm n-GaAs (1 μm/h, V/III = 15, Si-doped, 2 × 10¹⁸ cm⁻³), 20 nm n-Al$_{0.5}$Ga$_{0.5}$As (0.83 μm/h, V/III = 20, Si-doped, 2 × 10¹⁸ cm⁻³), and 200 nm n'-GaAs (0.5 μm/h, V/III = 30, Si-doped, 5 × 10¹⁸ cm⁻³). Nine more device stacks were grown by repeating the above-described steps and substrate temperature was kept at 610 °C throughout the growth of all device layers.

In characterization of materials properties and device performance at specific device stacks, overlying epitaxial layers were removed by repetitively etching device stack (in a mixture...
of phosphoric acid (85%, Fischer Scientific), hydrogen peroxide (H₂O₂, 30–32%, Macron), and deionized (DI) water (H₂O) with the volume ratio of 1:13:12 and sacrificial layers in diluted hydrofluoric acid (HF (48.5–50.5%, EMD):DI = 1:10 by volume). Microscale (≈500 × 500 μm²) GaAs solar cells on each device stack with a recessed bottom contact were fabricated by previously reported procedures. The photovoltaic performance was characterized using a semiconductor parameter analyzer (4156C, Agilent Technologies) and a full-spectrum solar simulator (94042A, Oriel). External and internal quantum efficiencies were obtained from QE measurement system (QEX7, PV Measurements). SIMS measurements were performed by a commercial vendor (EAG Laboratories).

### ASSOCIATED CONTENT

#### Supporting Information

The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsphotonics.8b00586.

SIMS concentration profiles of silicon and beryllium obtained from 1st, 2nd, 3rd, 4th, and 5th device stacks. Representative dark IV data measured from 1st, 5th, 7th, and 10th device stacks, with fitting curves by a single-diode equation (PDF).

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**Author Contributions**

J.Y. and M.L. conceived the idea and designed experiment. B.G., Y.S., H.C., M.L., and J.Y. performed the experiments and analyzed the data. B.G., Y.S., M.L., and J.Y. wrote the paper.

**Notes**

The authors declare no competing financial interest.

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### REFERENCES


